Table of Contents: Volume 6 (1993)

Number 1

Special Issue on VLSI Neural Networks
Guest Editor: Hans Peter Graf

Editorial ..... *Hans Peter Graf* 5
Recent VLSI Neural Networks in Japan ..... *Yuzo Hirai* 7
Recent Developments of Electronic Neural Nets in North America ..... *H.P. Graf, E. Sackinger, and L.D. Jackel* 19
Using Simulations of Reduced Precision Arithmetic to Design a Neuro-Microprocessor ..... *Krste Asanović, Nelson Morgan, and John Wawrzynek* 33
A General-Purpose Signal Processor Architecture for Neurocomputing and Preprocessing Applications ..... *Ulrich Ramacher, Jörg Beichter, and Nico Brüls* 45
A Mixed-Signal VLSI Competitive Neuroprocessor for Video Motion Detection ..... *Ji-Chien Lee, Bing J. Sheu, and Rama Chellappa* 57
Algorithmic and Implementation Issues in Analog Low Power Learning Neural Network Chips ..... *M. Jabri, S. Pickard, P. Leong, and Y. Xie* 67
Dynamic Adaptation of Quantization Thresholds for Soft-Decision Viterbi Decoding with a Reinforcement Learning Neural Network ..... *Yu-Jhih Wu, Michael D. Alston, and Paul M. Chau* 77
On Partitioning and Fault Tolerance Issues for Neural Array Processors ..... *Karl-Heinz Zimmermann, Tien-Chien Lee, and Sun-Yuan Kung* 85

Number 2

Special Issue on Field-Programmable Gate Arrays
Guest Editor: Will Moore and Wayne Luk

Introduction ..... *Will Moore and Wayne Luk* 99
Configurable Array Logic Circuits for Computing Network Error Detection Codes ..... *Gordon Brebner* 101
FIR Filters with Field-Programmable Gate Arrays ..... *Les Mintzer* 119
Quantitative Measurements of FPGA Utility in Special and General Purpose Processors ..... *Barry S. Fagin* 129
A Gate-Level Reconfigurable Monte Carlo Processor ..... *Sean Monaghan* 139
DSP System Integration and Prototyping with FPGAs ..... *Jouni Isoaho, Jari Pasanen, Olli Vainio and Hannu Tenhunen* 155
Using FPGAs to Implement Self-Timed Systems ..... *Erik Brunvand* 173
High Level Synthesis and Generating FPGAs with BEDROC System ..... *Miriam Leeser, Richard Chapman, Mark Aagaard, Mark Linderman, and Stephan Meier* 191

Number 3

VLSI Programmable Digital Filter for Video Signal Processing ..... *Giulio Casagrande, Armando Chiari, Carla Golla and Salvatore Miceli* 219
A Method for Calculation of the Square Root Using Combinatorial Logic .. *David M. Mandelbaum* 233
An Expandable Column FFT Architecture Using Circuit Switching Networks ..... *Tom Chen and Li Zhu* 243
A Superfast Algorithm for Single-Error Correction in RRNS and Hardware Implementation ..... *J.-D. Sun, Hari Krishna and K.-Y. Lin* 259
Scheduling Synchronous Dataflow Graphs for Efficient Looping ..... *Shuvra S. Bhattacharyya and Edward A. Lee* 271
Synthesis of Synchronous Communication Hardware in a Multiprocessor Architecture ..... *J.A. Huisken, A. Delaruelle, B. Egberts, P. Eeckhout and J. Van Meerbergen* 289